



PATENT
Docket No. 20002/17479

**IN THE UNITED STATES PATENT
AND TRADEMARK OFFICE**

Applicant(s): DESAI

Serial No.: 10/630,164

Filed: July 30, 2003

For: "Methods and Apparatus for
Maintaining Cache Coherency"

Group Art Unit: 2186

Examiner: Jonathan A. Barton

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) **April 24, 2006**

) 
) James A. Flight

) Registration No. 37,622

) Attorney for Applicant(s)

INFORMATION DISCLOSURE STATEMENT

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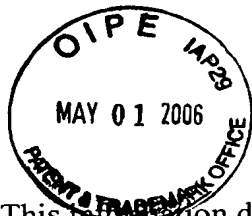
Dear Sir:

The documents listed on the enclosed PTO Form-1449 are submitted pursuant to
37 CFR §§ 1.56, 1.97, and 1.98. Copies of the non-U.S. Patent documents are enclosed.

05/01/2006 NNGUYEN1 00000101 10630164

03 FC:1806

180.00 0P



TIME OF FILING

This information disclosure statement is being filed to the best of the undersigned's knowledge, before the mailing date of a final action under 37 CFR §1.113 or notice of allowance under 37 CFR §1.311. Therefore, in accordance with 37 CFR §1.97(c), submitted herewith is the fee set forth in 37 CFR §1.17(p) for submission of an information disclosure statement under 37 CFR §1.97(c).

METHOD OF PAYMENT

Attached is a check in the amount of \$180.00

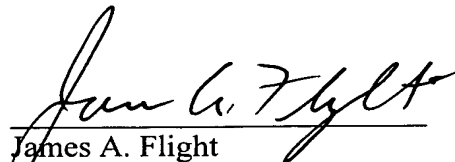
The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 50-2455. A copy of this paper is enclosed.

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Respectfully submitted,

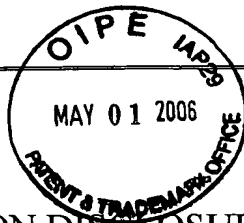
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By:


James A. Flight
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April 24, 2006

Form PTO-1449 (Modified)

U.S. Department of Commerce
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INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

U.S. PATENT DOCUMENTS

*EXAMINER INITIALS		DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	A01	5,664,150	09/1997	Isaac et al.			
	A02	5,765,199	06/1998	Chang et al.			
	A03	5,802,577	09/1998	Bhat et al.			
	A04	5,867,162	02/1999	O'Leary et al.			
	A05	5,913,226	06/1999	Sato			
	A06	6,266,744	07/2001	Hughes et al.			
	A07	6,425,060	07/2002	Mounes-Toussi et al.			
	A08	6,438,660	08/2002	Reams			
	A09	6,519,685	02/2003	Chang			
	A10	6,549,990	04/2003	Hughes et al.			
	A11	6,615,322	09/2003	Arimilli et al.			
	A12	6,615,323	09/2003	Petersen et al.			
	A13	6,694,409	02/2004	Chang			
	A14	6,775,748	08/2004	Jamil et al.			
	A15	5,996,049	11/30/99	Arimilli et al.			
	A16	5,943,684	08/1999	Arimilli et al.			
	A17	6,073,211	06/2000	Cheng et al.			
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	A20	6,360,301	03/2002	Gaither et al.			
	A21	6,378,048	04/2002	Prudvi et al.			
	A22	6,549,989	04/2003	Arimilli et al.			
	A23	6,574,710	06/2003	Gaither et al.			

EXAMINER

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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2186**U.S. PATENT DOCUMENTS**

*EXAMINER INITIALS		DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	A24	6,629,212	09/2003	Arimilli et al.			
	A25	6,574,710	06/2003	Gaither et al.			
	A26	6,785,774	08/2004	Arimilli et al.			
	A27	6,834,327	12/2004	Lyon			
	A28	6,321,297	11/2001	Shamanna et al.			
	A29	5,369,753	11/1994	Tipley			
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	A32	5,802,577	09/1998	Bhat et al.			
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	A34	6,266,744	07/2001	Hughes et al.			
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	A36	6,519,685	02/2003	Chang			
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	A39	5,512,874	04/1996	Poston, Travis			
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*EXAMINER INITIALS		DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	A47	6,552,578	04/2003	Cheung et al.			
	A48	6,593,801	07/2003	Hattori, Hide			
	A49	2003/0198296	10/2003	Bonelli et al.			
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	A61	6,167,492	12/2000	Keller et al.			
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	A63	6,405,289	06/2002	Arimilli et al.			
	A64	5,659,710	08/1997	Sherman et al.			
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	A66	2005/0166020	07/2005	Jamil et al.			

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		Filing Date July 30, 2003	Group Art Unit 2186

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

C01	Tomasevic, M; Milutinovic, V. "Hardware Approaches to Cache Coherence in Shared-Memory Multiprocessors, Part 1." IEEE Micro. Vol. 14, Issue 5, pp 52-59. Oct. 1994.
C02	Tomasevic, M; Milutinovic, V. "Hardware Approaches to Cache Coherence in Shared-Memory Multiprocessors, Part 2." IEEE Micro. Vol. 14, Issue 6, pp 61-66. Dec. 1994.
C03	"Intel® Itanium™ Processor Hardware Developer's Manual." ftp://download.intel.com/design/Itanium/Downloads/24870102.pdf. Document Number: 248701-002. August 2001.
C04	"Intel® Itanium™ 2 Processor Hardware Developer's Manual." ftp://download.intel.com/design/Itanium2/manuals/25110901.pdf. Document Number: 251109-001. July 2002.
C05	"Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Datasheet." ftp://download.intel.com/design/Pentium4/datashts/29864309.pdf. Document Number: 298643-009. May 2003.
C06	Handy, <i>The Cache Memory Book</i> , Academic Press, Inc., 2 nd edition, pp. 126-7; 156-186 (© 1998).
C07	Lee, <i>A Secondary Cache Controller Design for a High-End Microprocessor</i> , Institute of Electrical and Electronics Engineers, Inc., pp. 1141-1146 (© 1992).

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